IN THE CLAIMS

1. (Original) A computer system, comprising:

a central processing unit (CPU); and

at least one memory device coupled to the processor, the memory device including an array having memory cells arranged in rows and columns for storing a desired logic state, each cell including a first columnar structure and a spaced apart second columnar structure having a floating gate structure interposed between the first columnar structure and the second columnar structure and spaced apart from the first and second structures, the floating gate being positioned closer to a selected one of the first and second structures.

2. (Original) The computer system of claim 1, wherein the memory device further comprises a gate line positioned within the floating gate structure and electrically isolated from the floating gate structure, a first source/drain region and a second source/drain region coupling the first and second structures.

3. (Original) The computer system of claim 2, wherein the first and the second source/drain regions comprise a semiconductor material having a first conductivity.

4. (Original) The computer system of claim 3, further comprising a separation layer of a semiconductor material interposed between the first and second source/drain regions, the layer having a second conductivity.

5. (Original) The computer system of claim 3, wherein the first and the second source/drain regions comprise silicon and the first conductivity is an N+ conductivity.

6. (Original) The computer system of claim 4, wherein the separation layer comprises silicon and the second conductivity is a P- conductivity.

7. (Original) The computer system of claim 2, wherein the memory device further comprises a decoder coupled to each of the first source/drain region, the second source/drain region and the gate line.

8. (Original) The computer system of claim 7, further comprising an address buffer coupled to the decoders.

9. (Original) The computer system of claim 1, further comprising an address bus, a data bus and a control bus that couples the CPU to the at least one memory device.

10. (Original) The computer system of claim 9, further comprising a system controller coupled to the address bus, the data bus and the control bus.

11. (Original) The computer system of claim 10, further comprising at least one of a keyboard, a mouse, a display device and a modem coupled to the input/output module.

12. (Original) The computer system of claim 9, further comprising an external secondary mass storage device.

13. (Original) A semiconductor memory device, comprising:
an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance.

14. (Original) A semiconductor memory device, comprising:
an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance;

wherein each of the respective source/drain regions further comprise a first source/drain region and a spaced apart second drain region configured in a columnar structure extending upwardly from an underlying substrate, and further wherein a separation layer is interposed between the first source/drain region and the second drain region.

15. (Currently Amended) ~~The semiconductor memory device of claim 14,~~ A semiconductor memory device, comprising:

an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance;

wherein each of the respective source/drain regions further comprise a first source/drain region and a spaced apart second drain region configured in a columnar structure extending upwardly from an underlying substrate, and further wherein a separation layer is interposed between the first source/drain region and the second drain region; and

wherein the first source/drain region and the second drain region are comprised of a semiconductor material having an N+ conductivity, and further wherein the separation layer is comprised of a semiconductor material having a P- conductivity.

16. (Original) The semiconductor memory device of claim 13, wherein the common floating gate structure is comprised of polysilicon.

17. (Original) The semiconductor memory device of claim 13, wherein the second distance is approximately about two times the first distance.

18. (Original) The semiconductor memory device of claim 13, wherein the first distance is approximately about 30 Å.

19. (Currently Amended) ~~The semiconductor memory device of claim 13,~~ A semiconductor memory device, comprising:

an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions and a common floating gate structure that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance;

wherein the array further comprises a drain line extending in a first direction and coupling second source/drain regions of the first and second FETs, and further wherein the first source/drain region of the first and second FETs extend in a second direction that is perpendicular to the first direction.

20. (Original) The semiconductor memory device of claim 19, wherein the array further comprises a gate line that extends in the second direction.

21. (Original) The semiconductor device of claim 20, further comprising a decoder coupled to each of the drain line, the first source/drain region and the gate line.

22. (Original) A method of forming a memory device having a plurality of interconnected memory cells, each cell comprising:

positioning a first columnar structure on a substrate;

positioning a second columnar structure on the substrate that is spaced apart from the first columnar structure;

forming a gate structure between the first structure and the second structure; and

interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure, the floating gate structure being positioned closer to selected one of the first structure and the second structure.

23. (Currently Amended) ~~The method of claim 22,~~ A method of forming a memory device having a plurality of interconnected memory cells, each cell comprising:

positioning a first columnar structure on a substrate;

positioning a second columnar structure on the substrate that is spaced apart from the first columnar structure;

forming a gate structure between the first structure and the second structure; and

interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure, the floating gate structure being positioned closer to selected one of the first structure and the second structure;

wherein positioning a first and second columnar structures on the substrate further comprises positioning the first and second columnar on a silicon substrate that is doped to have a first conductivity.

24. (Original) The method of claim 23, wherein positioning the first and second columnar on a silicon substrate that is doped to have a first conductivity includes doping the substrate to have a P conductivity.

25. (Original) The method of claim 22, wherein positioning a first and second columnar structures on the substrate further comprises:

forming a first source/drain region having a first conductivity on the substrate;

forming a second source/drain region proximate to the first source/drain region, the second source/drain region having the first conductivity; and

interposing a separation layer between the first source/drain region and the second source/drain region.

26. (Original) The method of claim 25, wherein forming a first source/drain region having a first conductivity comprises forming a source/drain region having an N+ conductivity.

27. (Currently Amended) ~~The method of claim 25,~~ A method of forming a memory device having a plurality of interconnected memory cells, each cell comprising:

positioning a first columnar structure and a second columnar structure on the substrate that is spaced apart from the first columnar structure, wherein positioning a first and second columnar structures on the substrate further comprises,

forming a first source/drain region having a first conductivity on the substrate,

forming a second source/drain region proximate to the first source/drain region, the second source/drain region having the first conductivity, and

interposing a separation layer between the first source/drain region and the second source/drain region;

forming a gate structure between the first structure and the second structure; and

interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure, the floating gate structure being positioned closer to selected one of the first structure and the second structure;

wherein forming a second source/drain region proximate to the first source/drain region comprises forming a source drain region having an N+ conductivity above the second source/drain region.

28. (Original) The method of claim 25, wherein interposing a separation layer between the first source/drain region and the second source/drain region comprises forming a layer between the first source/drain region and the second source/drain region having a second conductivity.

29. (Original) The method of claim 28, wherein forming a layer between the first source/drain region and the second source/drain region having a second conductivity comprises forming a layer that is doped to a P- conductivity between the first source/drain region and the second source/drain region.

30. (Original) The method of claim 22, wherein interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure further comprises positioning an insulating layer between the floating gate structure and the first and second columnar structures.

31. (Original) The method of claim 30, wherein positioning an insulating layer between the floating gate structure and the first and second columnar structures comprises forming a first insulating layer between the first structure and the floating gate structure having a first thickness and forming a second insulating layer between the second structure and the

floating gate structure having a second thickness, the first thickness being less than the second thickness.

32. (Original) The method of claim 25, further comprising coupling the second source/drain region of the first columnar structure and the second source/drain region of the second columnar structure with a drain line.